Physical Design with Timing Precision of 4-Bit Counter for Cyber Physical Systems

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Abstract

This paper presents the importance of an optimized physical design for a 4-bit counter in enhancing cryptographic operations within Cyber-Physical Systems (CPS). Key design aspects, including timing precision, power efficiency, and area optimization, are explored. The 4-bit counter with accurate clock tree synthesis provides precise timing control, ensuring synchronized data transfer essential for secure encryption and decryption processes. In energy-sensitive CPS applications, such as smart meters, power-efficient counter designs minimize switching activities, reducing dynamic power consumption and supporting prolonged operational lifetimes. Additionally, the compact layout of an area-optimized counter conserves valuable silicon space, enabling integration with critical cryptographic modules without compromising device performance or security. This work underscores the role of efficient physical design in advancing secure, reliable, and resource-constrained CPS environments.

Keywords: Cyber-Physical Systems (CPS),4-bit Counter Design, Timing Precision, Power Efficiency, Area Optimization, Cryptographic Operations

1. Introduction

In Cyber-Physical Systems (CPS), such as smart meters, autonomous vehicles, and industrial control systems, secure and efficient cryptographic operations are essential to protect data integrity and privacy [1]. However, CPS devices often face stringent resource constraints, requiring careful optimization in hardware design to ensure reliable performance without excessive power consumption or space usage [2].

A critical component in many cryptographic processes within CPS is the 4-bit counter, which serves functions such as key generation, timing control, and data synchronization. The physical design of this counter directly impacts the system's overall efficiency and security. Precision in timing and synchronization, achieved through accurate clock tree synthesis, is crucial for ensuring that cryptographic operations remain aligned with system requirements [3]. Power efficiency is equally vital, especially in energy-sensitive applications, as it enables prolonged operation and reduces the risk of side-channel attacks that may exploit power fluctuations [4]. Furthermore, optimizing the counter's area footprint is necessary to conserve silicon space, thereby allowing the integration of additional cryptographic modules without compromising system performance or security [5].

This paper examines the influence of timing precision, power efficiency, and area optimization in the physical design of a 4-bit counter, highlighting its significance in supporting secure and resilient cryptographic operations in resource-limited CPS environments [6].

This research is structured as follows: Section 2 presents the proposed work, detailing the specific methodology and design approach used to enhance timing precision, power efficiency, and area optimization in the 4-bit counter. Section 3 explores the significance of timing precision and synchronization in the design of a 4-bit counter for cryptographic operations within Cyber-Physical Systems (CPS). Section 4 examines the power efficiency requirements in CPS applications, Section 5 discusses on how an optimized counter design supports secure operations in energy-sensitive environments. Section 6 provides a detailed analysis of the results and performance improvements achieved by the proposed design. Finally, Section 7 concludes the paper with a summary of key findings and proposes potential directions for future research to further advance secure, resource-efficient counters for CPS.

2.Proposed Work

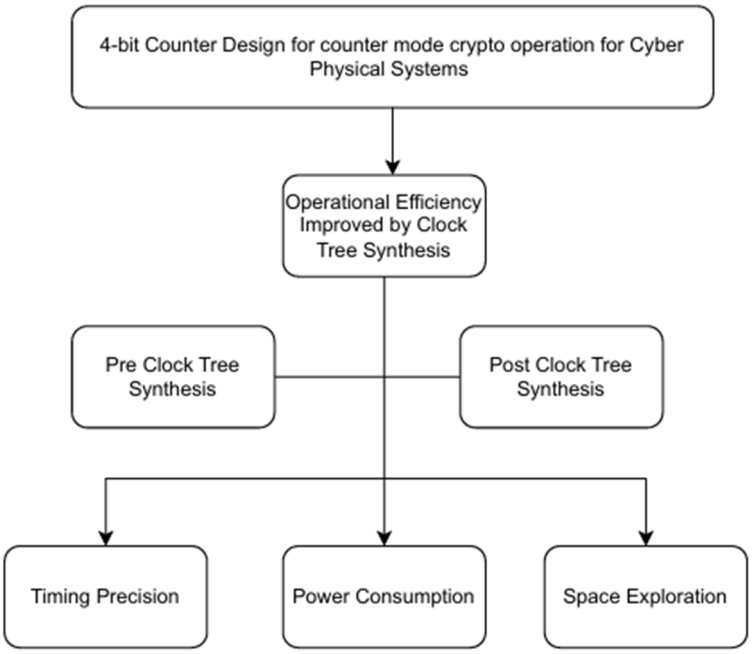

Fig.1 Methodology for 4-bit Counter Design with Timing Precision

Clock Tree Synthesis (CTS) plays a crucial role in digital design, particularly in Cyber-Physical Systems (CPS), by ensuring reliable and precise timing performance as mentioned in Figure.1. Here's a detailed look at why CTS is essential for this work:

Reducing Clock Skew

- **Definition**: Clock skew refers to the variation in arrival times of the clock signal at different parts of the circuit.
- **Significance**: In high-speed and synchronous digital circuits, even minor skew can cause timing violations, potentially leading to data errors and system instability.
- **CTS Function**: CTS balances the distribution of the clock signal across the circuit, reducing skew and ensuring that all components receive the clock pulse nearly simultaneously—an essential requirement for stable CPS operation.

Achieving Consistent Timing

- **Challenge**: In large, interconnected designs, timing discrepancies may arise due to physical distance and variations in path delays.
- **CTS Solution**: By generating a clock network that meets timing requirements across all paths, CTS ensures timing consistency, which is critical in CPS for accurate data processing and real-time functionality.

Enhancing Performance and Managing Clock Latency

- **Performance Demands**: Many CPS applications require high-speed operation, especially in real-time systems where excessive clock latency can reduce efficiency.
- **CTS Advantage**: CTS minimizes clock latency by designing an optimized clock distribution network, which reduces the delay from the clock source to various parts of the circuit, thus enhancing overall design performance.

Lowering Dynamic Power Consumption

- **Power Requirements**: Energy-sensitive CPS applications, like smart meters, need to minimize power consumption. Since clock networks contribute significantly to dynamic power due to frequent switching, optimization is crucial.
- **CTS Benefit**: By creating a balanced and efficient clock tree with effective clock gating, CTS reduces unnecessary toggling in inactive parts of the circuit, minimizing dynamic power consumption and supporting longer operational life for CPS devices.

Preserving Signal Integrity

- **Issue**: High-frequency clock signals can experience noise and coupling effects, which degrade signal integrity and risk data corruption.
- **CTS Solution**: CTS carefully routes the clock signal to reduce interference and maintain signal quality, which is vital for data accuracy and system reliability in CPS applications.

Facilitating Scalability and Managing Complexity

- **Scalability**: As design complexity increases, managing clock distribution without CTS becomes highly challenging.
- **CTS Advantage**: CTS automates clock distribution, making it easier to scale designs and integrate new components. In CPS, which often requires scalability and adaptability, CTS ensures that the system's performance remains robust as complexity grows.

3.Timing Precision and Synchronization

This 4bit Counter is designed with clock frequency of 100 MHz and amplitude of 1V, maximum input delay 1.0 ns, maximum output delay of 1.0 ns, rise clock transition 0.1 V, fall clock transition 0.1V

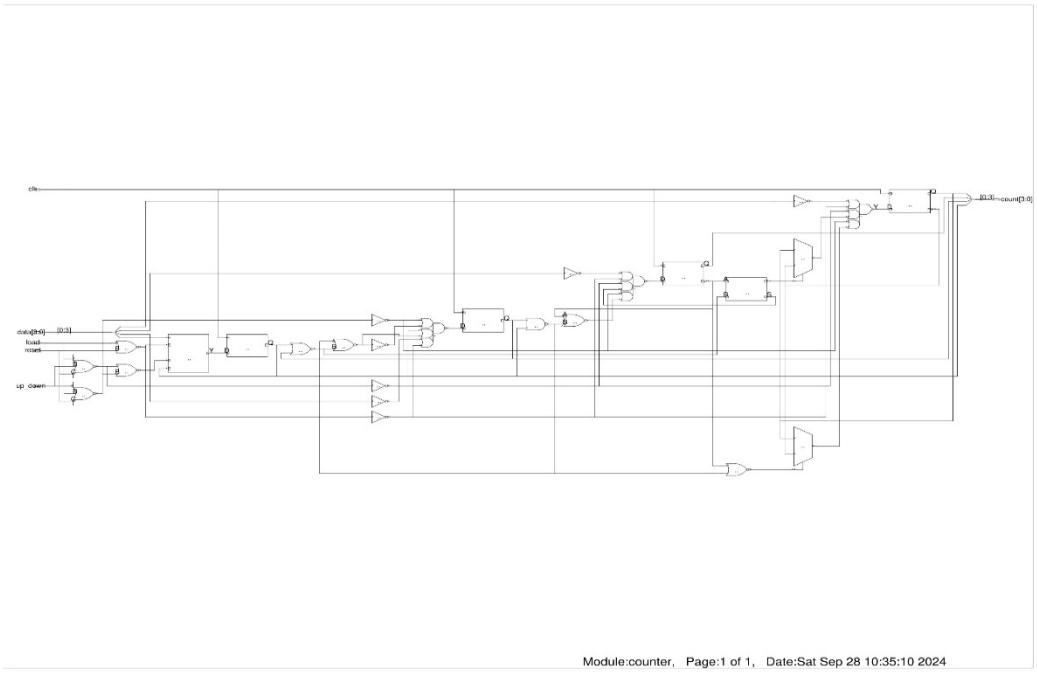

Fig.2.Schematic Diagram of 4-bit Counter for Counter mode crypto Operation

```
ncsim>
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm counter_tb.clk counter_tb.count counter_tb.data counter_tb.load counter_tb.reset
Created probe 1
ncsim> run
time=0,  reset=1,  load=x,  data= 8,  count= x
time=3,  reset=1,  load=x,  data= 8,  count= 0
time=7,  reset=0,  load=x,  data= 8,  count= 0
time=9,  reset=0,  load=x,  data= 8,  count=15
time=12,  reset=0,  load=1,  data= 8,  count=15
time=14,  reset=0,  load=1,  data=13,  count=15
time=15,  reset=0,  load=1,  data=13,  count=13
time=16,  reset=0,  load=1,  data=15,  count=13
time=17,  reset=0,  load=0,  data=15,  count=13
time=21,  reset=0,  load=0,  data=15,  count=12
time=27,  reset=0,  load=0,  data=15,  count=11
time=33,  reset=0,  load=0,  data=15,  count=10
time=39,  reset=0,  load=0,  data=15,  count= 9
time=42,  reset=1,  load=0,  data=15,  count= 9
time=45,  reset=1,  load=0,  data=15,  count= 0
```

Fig.3. Behavioural Simulation of 4-bit counter

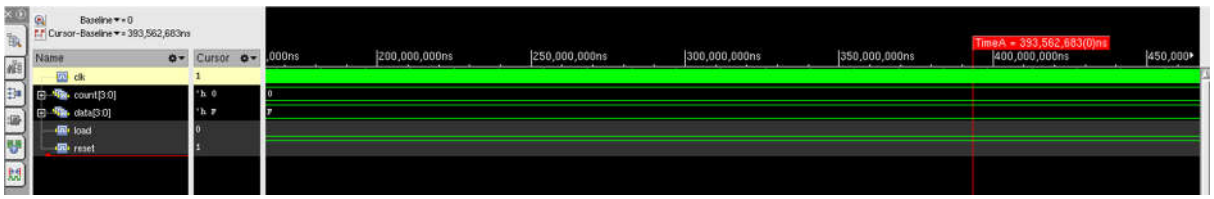

Fig.4. Waveform output of 4bit counter

```
====================================================================
  Generated by:           Encounter(R) RTL Compiler v14.10-s022_1
  Generated on:           Oct 23 2024  09:49:00 am
  Module:                 counter
  Technology library:     fast
  Operating conditions:   fast (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================

             Pin                      Type      Fanout Load Slew Delay Arrival
                                                     (fF) (ps)  (ps)   (ps)
--------------------------------------------------------------------------------
(clock clk)                          launch                                0 R
count_reg[0]/CK                                          100                0 R
count_reg[0]/Q                       DFFQX2          4 12.4   46  +115     115 F
count[0]                             out port                    +0     115 F
(constraints_timing.s_line_6_3_1)    ext delay                  +1000    1115 F
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock clk)                          capture                              2000 R
--------------------------------------------------------------------------------
Cost Group   : 'clk' (path_group 'clk')
Timing slack :     885ps
Start-point  : count_reg[0]/CK
End-point    : count[0]
```

Fig.5. Report of Timing Precision while Synthesis of Design

Figure 1 presents the schematic diagram of the 4-bit counter. Figure 2 illustrates the counting progress over time based on the design. Figure 3 shows the waveform representing the counter's behaviour, while Figure 5 depicts the timing precision of the counter. The timing parameters indicate that the design is well-suited for operation at

100 MHz with a delay and arrival time of 115 ps, the circuit shows minimal internal delay, aligning well with the 10 ns clock period, which helps prevent timing violations. A fanout of 4 and a load of 12.4fF suggest the output load is moderate, allowing the design to maintain its speed without significant delay. The slew rate of 100 ps provides quick signal transitions, preserving signal integrity in a high-frequency environment. Additionally, the 46 ps output register delay supports efficient timing synchronization. Overall, the design appears optimized for stable and accurate performance at 100 MHz.

4.Power Efficiency Requirements for CPS

```
============================================================
  Generated by:           Encounter(R) RTL Compiler v14.10-s022_1
  Generated on:           Oct 23 2024  09:49:00 am
  Module:                 counter
  Technology library:     fast
  Operating conditions:   fast (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

                Leakage   Dynamic    Total
Instance Cells Power(nW) Power(nW) Power(nW)
------------------------------------------------
counter     27    18.497 71048.669 71067.166
```

Fig.6. Report of Power requirement for the Proposed Design

Reducing Power Consumption: Minimize both dynamic (switching) and static (leakage) power by employing energy-saving strategies like clock gating, voltage reduction, and standby modes to cut down unnecessary power usage.

Enhancing Algorithm Efficiency: opt for computationally efficient algorithms to lower processing demand. For cryptographic operations, using algorithms that require fewer steps or lightweight cryptography methods can significantly reduce power usage.

Effective Power Management: Apply dynamic power management techniques such as adaptive voltage and frequency scaling (DVFS) to adjust power levels according to the current workload.

Selecting Low-Power Components: Choose components like low-power FPGAs or microcontrollers with energy-saving features, ensuring they align with the specific power needs of the application.

Managing Heat Dissipation: Ensure proper cooling and thermal management to sustain performance while preventing additional power loss due to heat-induced throttling.

With a total power consumption of 71,067 nW at 100 MHz, your design primarily uses dynamic power (71,048 nW) during active operation, with only a small portion (18 nW) as leakage power when idle. This low leakage indicates good idle power control, making the design efficient. Since over 99% of the power is dynamic, applying techniques like clock gating or algorithmic adjustments could further improve efficiency. Overall, the total power

of 71,067 nW (or 71.067 nW) at 100 MHz is low and suitable for many low-power applications, meeting typical power requirements in similar designs illustrates in Figure 6.

```
  output [3:0] count;
  wire clk, reset, up_down, load;
  wire [3:0] data;
  wire [3:0] count;
  wire n_0, n_2, n_4, n_7, n_20, n_23, n_24, n_25;
  wire n_26, n_27, n_28, n_30, n_32, n_33, n_35, n_36;
  wire n_37, n_38, n_39, n_40, n_41, n_42, n_55, n_56;
  wire n_57, n_58;
  DFFQX2 \count_reg[1] (.CK (clk), .D (n_41), .Q (count[1]));
  OAI222X2 g425(.A0 (n_0), .A1 (n_38), .B0 (n_39), .B1 (n_36), .C0
       (n_40), .C1 (n_35), .Y (n_42));
  OAI222X2 g433(.A0 (n_40), .A1 (n_32), .B0 (n_39), .B1 (n_56), .C0
       (n_2), .C1 (n_38), .Y (n_41));
  OAI222X2 g427(.A0 (n_4), .A1 (n_38), .B0 (n_39), .B1 (n_28), .C0
       (n_40), .C1 (n_55), .Y (n_37));
  DFFQX2 \count_reg[0] (.CK (clk), .D (n_30), .Q (count[0]));
  MXI2X1 g431(.A (count[3]), .B (n_33), .S0 (n_27), .Y (n_36));
  MXI2X1 g430(.A (count[3]), .B (n_33), .S0 (n_25), .Y (n_35));
  CLKINVX2 g438(.A (n_56), .Y (n_32));
  OAI2BB2X1 g432(.A0N (data[0]), .A1N (n_57), .B0 (n_23), .B1
       (count[0]), .Y (n_30));
  ADDHX1 g434(.A (n_7), .B (n_26), .CO (n_27), .S (n_28));
  NOR2X1 g437(.A (n_7), .B (n_24), .Y (n_25));
  NOR2X1 g435(.A (n_20), .B (n_58), .Y (n_23));
  CLKINVX4 g440(.A (n_58), .Y (n_40));
  NAND2X6 g448(.A (count[1]), .B (count[0]), .Y (n_24));
  CLKINVX4 g442(.A (n_20), .Y (n_39));
  CLKINVX4 g444(.A (n_57), .Y (n_38));
  NOR2X8 g446(.A (count[0]), .B (count[1]), .Y (n_26));
  NOR3X8 g443(.A (load), .B (up_down), .C (reset), .Y (n_20));
  INVXL g458(.A (data[2]), .Y (n_4));
  INVXL g468(.A (data[1]), .Y (n_2));
  INVXL g459(.A (data[3]), .Y (n_0));
  XNOR2X4 g2(.A (n_7), .B (n_24), .Y (n_55));
  DFFX4 \count_reg[3] (.CK (clk), .D (n_42), .Q (count[3]), .QN (n_33));
  DFFX4 \count_reg[2] (.CK (clk), .D (n_37), .Q (count[2]), .QN (n_7));
  NOR2BX4 g478(.AN (n_24), .B (n_26), .Y (n_56));
  NOR2BX4 g479(.AN (load), .B (reset), .Y (n_57));
  NOR3BX4 g480(.AN (up_down), .B (load), .C (reset), .Y (n_58));
endmodule
```

Fig.7. Netlist Creation of Counter 4bit Design

Figure 7 and 8 shows that the creation of a 27-cell netlist represents a synthesized design where the circuit is mapped to 27 individual logic cells. Each cell in the netlist corresponds to a specific functional unit, such as logic gates (AND, OR, NOT) or storage elements (flip-flops), based on the high-level design. During synthesis, the tool optimizes the design by minimizing the number of cells while meeting design constraints for timing, power, and area. This optimized 27-cell configuration not only simplifies the circuit but also enhances power efficiency and

performance, making it ideal for compact, low-power applications where both functionality and resource management are essential.

```
============================================================
  Generated by:           Encounter(R) RTL Compiler v14.10-s022_1
  Generated on:           Oct 23 2024  09:49:00 am
  Module:                 counter
  Technology library:     fast
  Operating conditions:   fast (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Instance  Cells  Cell Area  Net Area  Total Area  Wireload
------------------------------------------------------------
counter      27          0         0           0    <none> (D)

 (D) = wireload is default in technology library
```

Fig.8. Report of Area for counter design

5.Optimized Counter Design

```
add_ndr -width {Metal1 0.12 Metal2 0.14 Metal3 0.14 Metal4 0.14 Metal5 0.14 Metal6 0.14 Metal7 0.14 Metal8 0.14 Metal9 0.14 } -spacing {Metal1 0.12 Metal2 0.14 Metal3 0.14 Metal4 0.14 Metal5
0.14 Metal6 0.14 Metal7 0.14 Metal8 0.14 Metal9 0.14 } -name 2w2s
create_route_type -name clkroute -non_default_rule 2w2s -bottom_preferred_layer Metal5 -top_preferred_layer Metal6
set_ccopt_property route_type clkroute -net_type trunk
set_ccopt_property route_type clkroute -net_type leaf
set_ccopt_property buffer_cells {CLKBUFX8 CLKBUFX12}
set_ccopt_property inverter_cells {CLKINVX8 CLKINVX12}
set_ccopt_property clock_gating_cells TLATNTSCA*
create_ccopt_clock_tree_spec -file ccopt.spec
```

Fig.9 Script to perform Clock Tree Synthesis for optimization

Figure 9 illustrates a script designed to perform Clock Tree Synthesis (CTS) for optimization in the context of a digital circuit design. Clock Tree Synthesis is a critical step in the physical design process, where the goal is to distribute the clock signal evenly across the entire circuit to ensure proper timing and synchronization. The script automates the process by generating the clock tree structure, optimizing the distribution of clock signals to minimize skew (the difference in arrival times of the clock signal at different parts of the circuit), reduce power consumption, and improve signal integrity.

6.Result and Analysis

The proposed work focuses on designing an optimized 4-bit counter to improve cryptographic operations in Cyber-Physical Systems (CPS). This work aims to enhance three key aspects: timing precision, power efficiency, and area optimization. The design employs accurate clock tree synthesis to ensure precise timing control and synchronization for cryptographic processes.

In summary, CTS is a key process that meets the goals of CPS design by providing precise timing, optimizing power use, and ensuring stable, high-speed performance. By building an efficient and balanced clock network in Figure 10, CTS enables CPS applications to meet demanding operational standards and maintain reliability, especially in real-time settings.

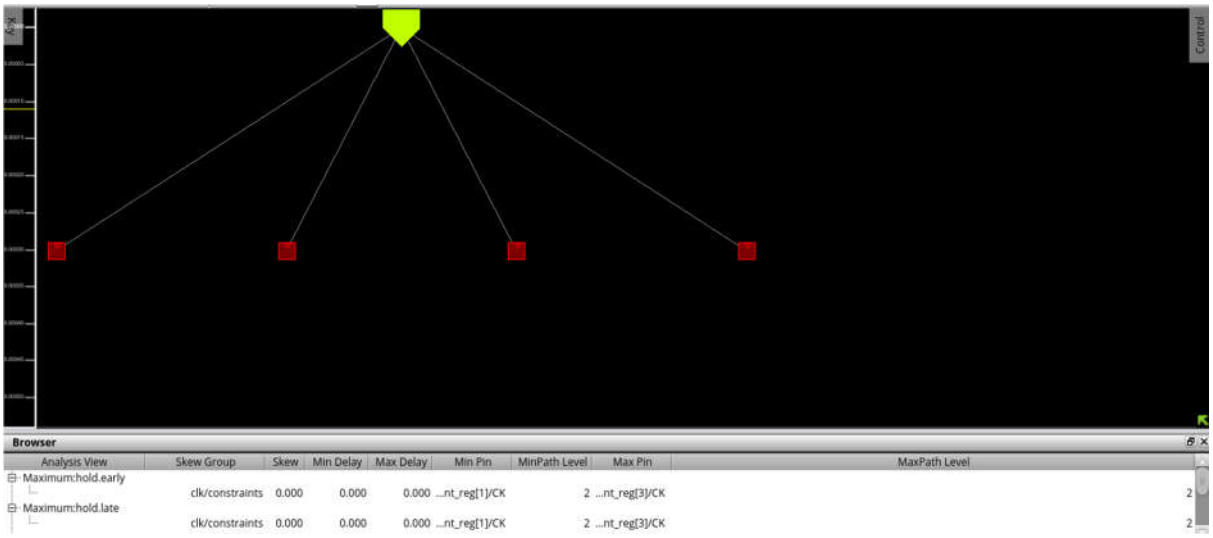

Fig.10. Clock Tree Synthesis of 4-bit counter design

6.1 Pre-CTS Reports

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 worst

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.029  |  0.870  |  0.029  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    8    |    4    |    8    |
+--------------------+---------+---------+---------+
```

Fig.11. PreCTS Setup mode Timing Precision

```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

Setup views included:
 worst

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.086  |  0.964  |  0.086  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    8    |    4    |    8    |
+--------------------+---------+---------+---------+
```

Fig.12. PreCTS setup mode optimized design

6.2 Post CTS Reports

```
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 worst

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.154  |  0.988  |  0.154  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    8    |    4    |    8    |
+--------------------+---------+---------+---------+
```

Fig.13. Post CTS setup mode timing precision

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 best

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.017  |  0.123  |  0.017  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    4    |    4    |    4    |
+--------------------+---------+---------+---------+
```

Fig.14. Post CTS hold mode timing precision

```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

Setup views included:
 worst
Hold  views included:
 best

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.086  |  0.964  |  0.086  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    8    |    4    |    8    |
+--------------------+---------+---------+---------+

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.017  |  0.123  |  0.017  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    4    |    4    |    4    |
+--------------------+---------+---------+---------+
```

Fig.15. Post CTS optimized design timing precision

By analysing Figures 11 to 15, the report on Clock Tree Synthesis in various modes shows that the final post-CTS optimized design demonstrates an improvement in the worst negative slack between registers in both setup and hold modes, making it well-suited for counter mode cryptographic operations in Cyber-Physical Systems.

7.Conclusion with Future work

This research emphasizes the importance of an optimized 4-bit counter design to improve cryptographic operations in Cyber-Physical Systems (CPS). By focusing on timing precision, power efficiency, and space optimization, the proposed design addresses key challenges in CPS, especially in resource-limited devices like smart meters and IoT sensors. Accurate timing helps keep cryptographic processes synchronized, while a power-efficient design supports longer operation in energy-sensitive environments. The compact design also conserves silicon space, allowing more secure components to fit on the device. The results show that a well-designed 4-bit counter can greatly enhance both security and efficiency in CPS. Future work could explore ways to make the counter even more secure or adaptable to different cryptographic needs. This study highlights how optimized hardware design can support the growing demands of secure and efficient Cyber-Physical Systems.

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